REMARKS

Claims 1, 13, 20 and 22 have been amended. Claim 16 has been canceled without prejudice or disclaimer and new claim 24 has been added. Accordingly, claims 1, 5-9, 13-15, 20-22 and 24 are pending.

Claims 1, 5, 6, 8, 9, 13, 14, 20 and 21 stand rejected under 35 U.S.C. §103 as being unpatentable over Ikeda et al in view of Asano et al and further in view of Fleisher. Further, claim 22 is rejected over the Bjornbahl et al reference under 35 U.S.C. §103(a) and claim 13 is rejected as being anticipated by Kiani-Shabestari et al under 35 U.S.C. §102(b). Reconsideration of the rejections is requested for the following reasons.

Claim 1 has been amended to set forth that the plurality of switching LSI's are capable of programming connections between the plurality of programmable LSI's. Further, each of independent claims 1, 13, and 20 have been amended to include that each of the plurality of programmable LSI's is directly connected to all of the other of the plurality of programmable LSI's and is coupled to all of the plurality of switching LSI's. As amended, each of claims 1, 13, and 20 avoids the Ikeda, Asano and Fleisher references since none of these references discloses each of the plurality of programmable logic elements being directly connected to all of the other of

the plurality of programmable logic elements and being coupled to all of the switching elements.

The Examiner notes in the Office Action that Ikeda does not explicitly show lines from connectors to programmable LSI's and the linking of programmable LSI's by way of switching LSI's. Applicants note further that, as shown in Fig. 6 of Ikeda, the emulation FPGA 3 cannot output/input signals to/from the emulation FPGA 4. Accordingly, the reference does not teach that each of the plurality of programmable logic elements is directly connected to all of the other of the programmable logic elements and further coupled to all of the switching elements, as claimed.

Asano is relied upon in the Office Action for disclosing a programmable logic emulation system having programmable LSI's connected via field programmable logic arrays. However, as shown in Fig. 7 of Asano, for example, the emulation chips in each stage cannot output/input signals to/from each other. Accordingly, the reference does not make up for the deficiencies in Ikeda noted by Applicants with respect to the reference's failure to disclose and/or suggest the invention of amended claims 1, 13, and 20.

Fleisher is cited for the use of stacking type connectors in emulation modules. However, Fleisher does not disclose the aspect of the invention set forth in amended claims 1, 13, and

20 with respect to each of the plurality of programmable logic elements being directly connected to all of the other plurality of programmable elements and being coupled to all of the switching elements. Accordingly, the combination of Ikeda, Asano and Fleisher does not render the invention unpatentable under 35 U.S.C. §103(a), and therefore the rejection should be withdrawn.

As amended, claim 13 overcomes the 35 U.S.C.§102(b) rejection based on Kiani-Shabestari et al. The reference is relied upon for disclosing a programmable logic emulation system having programmable LSI's connected via PLA's, however, the reference does not disclose that each of the plurality of programmable logic elements is directly connected to all of the other of the programmable logic elements and coupled to all of the switching elements. Therefore, the 35 U.S.C. §102(b) rejection should be withdrawn.

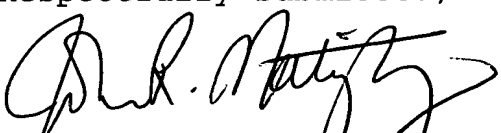
Claim 22 has been amended to overcome the 35 U.S.C. §103(a) rejection using Bjorndahl et al. Bjorndahl is relied upon for disclosing a multi chip module with integrated circuits and radiation plates on both sides of the module. However, amended claim 22 sets forth that the first and second radiation plates are attached to the four corners of the multi chip module, and that first metal spacers are interposed between the first radiation plates and the first side of the

board and second metal spacers are interposed between the second radiation plate and a second side of the board. Further, first and second heat conduction sheets are claimed which are interposed between the integrated circuits mounted on the first and second sides of the board and the first and second radiation plates, respectively. Therefore, claim 22 is not anticipated by Kiani-Shabestari et al and accordingly the 35 U.S.C. §102(b) rejection should be withdrawn.

Claim 24 has been added and is dependent on claim 13. Accordingly, claim 24 should be allowed for depending from an allowable base claim. Similarly, each of the dependent claims should now be found to be allowable at least for depending from an allowable base claim.

In view of the foregoing amendments and remarks, reconsideration and reexamination are respectfully requested.

Respectfully submitted,



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